Reverse battery protection for the nPM2100 PMIC

Guideline

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Contents

Revision history

Date	Description
March 2026	First release

1 Introduction

Most devices that are powered by a non-rechargeable battery require the user to replace that battery. The device should be protected from accidental reverse battery installation. This means that designers of battery-powered devices should consider the effects of reverse polarity and make sure the battery or the device itself is not damaged if the battery is installed in reverse polarity.

Protection methods can be either mechanical or electrical. Mechanical protection methods include instruction symbols and battery holders which allow the insertion of the battery only in one direction. Certain battery types can be more difficult to protect from reverse battery polarity by mechanical means. In these cases, electrical protection methods are needed.

These guidelines present different protection methods for nPM2100 PMIC use cases and the main considerations for each approach.

2 Operation without protection

The nPM2100 PMIC does not have an internal battery protection mechanism. This means that if a battery is inserted in reverse polarity, the voltage of the battery is clamped to about 0.6 V due to the nPM2100 PMIC's internal *Electrostatic Discharge (ESD)* protection structure. This causes the battery and the nPM2100 PMIC to heat up. Long-term exposure to this condition can damage the nPM2100 PMIC, the battery, or both.

3 Battery types

Battery form factor, voltage, and internal resistance are all factors that should be considered when selecting a suitable protection method. The following are typical battery types to be used in an nPM2100 application and the main considerations for each option.

1.5 V batteries

- AA and AAA alkaline batteries have very low internal resistance. This means that when installed in reverse, currents can be high and cause damage to the device or overheat the battery.
- Low voltage makes it difficult to control the protection *Field-Effect Transistor (FET)*, especially when the battery is discharged and voltage drops.
- Low voltage makes it difficult to add a diode in series since it causes a voltage drop and reduces usable battery capacity and overall efficiency.
- LR41 and LR44 batteries have a relatively high internal resistance. When installed in reverse, this can reduce the short-circuit current which improves safety.

3 V batteries

- CR batteries typically have a relatively high internal resistance. This limits the short-circuit current, but results in lower *Equivalent Series Resistance (ESR)* and higher currents when physically larger higher-capacity battery form factors are used.
- Two AA or AAA batteries in series have low internal resistance and high capacity. When installed in reverse, this increases the likelihood of overheating and damage to the nPM2100 PMIC.
- Higher voltage makes the protection FET easier to control, and even a diode in series can be considered in some cases.

Summary of battery options

Parameter	Single AA or AAA	Two AA or AAA in series	LR44	CR2032
Open circuit voltage (V)	0.8 to 1.6	1.6 to 3.2	0.9 to 1.6	2.0 to 3.2
ESR (Ω)	< 1	< 2	15 to 20	10 to 80

Table 1: Summary of battery options

4 Protection with a FET

A common way to protect a device from a reverse current is using a *FET*. The FET is used either as a *P-Channel Metal-Oxide-Semiconductor (PMOS)* on the battery's positive side or as an *N-Channel Metal-Oxide-Semiconductor (NMOS)* on the negative side.

Especially when operating with a 1.5 V battery, the gate-source voltage threshold of the selected FET is critical. It must be low enough to be able to turn on the FET even when the battery is in a low state of charge.

4.1 PMOS

When the battery is installed in reverse polarity, the gate voltage of the *PMOS FET* is high which prevents it from turning on. When the battery is installed in the correct polarity, the gate voltage of the PMOS FET is pulled low, and it switches on.

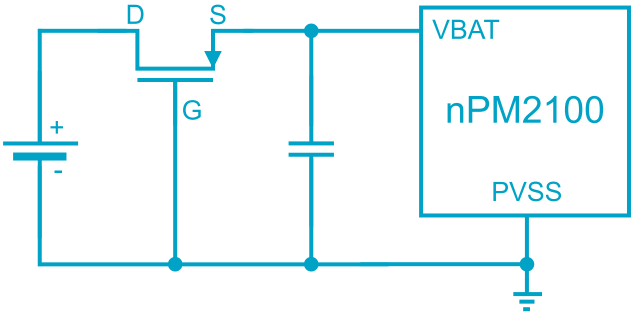

Figure 1: PMOS connection diagram

When the PMOS FET is used, a voltage drop appears between the drain and source. The drop is equal to $R_{DS(on)}$ × IBAT, where $R_{DS(on)}$ is the drain-source on-resistance. The gate itself has a very high impedance, and virtually no extra quiescent current is drawn through the gate connection.

For performance testing, an Analog Power AM2305PE FET was used since its gate-source voltage is low enough, its current rating is sufficient for the nPM2100 application, and its $R_{DS(on)}$ is low enough to allow a low voltage drop across the FET in normal operation. Also, its package size is SOT-23, which is relatively small.

4.2 NMOS

When the battery is installed in reverse polarity, the gate voltage of the *NMOS FET* is low which prevents it from turning on. When the battery is installed in the correct polarity, the gate voltage of the NMOS FET goes high, and it switches on.

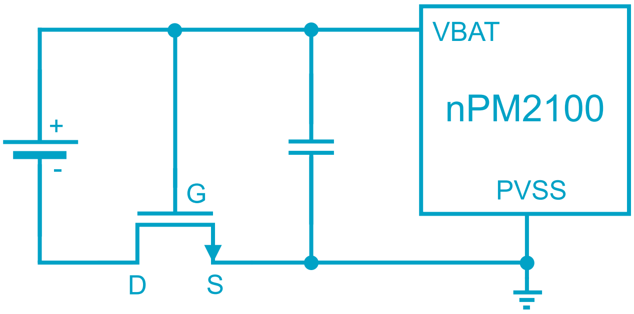

Figure 2: NMOS connection diagram

When the NMOS FET is used, a voltage drop appears in the ground return path. The drop is equal to $R_{DS(on)}$ × IBAT, where $R_{DS(on)}$ is the drain-source on-resistance. The gate itself has a very high impedance, and virtually no extra quiescent current is drawn through the gate connection.

For performance testing, an Analog Power AM2336N FET was used since its gate-source voltage is low enough, its current rating is sufficient for the nPM2100 application, and its $R_{DS(on)}$ is low enough to allow a low voltage drop across the FET in normal operation. Also, its package size is SOT-23, which is relatively small.

4.3 Startup considerations

An nPM2100 EK with default components was used to test the behavior of the added *PMOS* and *NMOS* in series with the battery. The effect on the minimum startup voltage depends on the *FET* used.

When an AM2305PE or AM2336N FET is used, the nPM2100 PMIC boost converter turned on with a minimum startup voltage of 0.86 V. This is slightly higher than the specified cold-start minimum voltage of 0.8 V.

4.4 System efficiency and maximum load considerations

The type of *FET* used and the battery voltage influence the system efficiency and maximum achieved load current.

Especially when operating at low voltages, the FET's gate-source voltage is not enough to fully turn it on. This results in voltage drops across the transistor, which reduces the overall efficiency.

Input capacitance also has an effect, especially when boost is operating in hysteretic mode. A higher input capacitance results in a lower peak current across the FET during boost activity. This helps in reducing $I^2 \times R$ losses at the expense of board real estate and BOM cost.

1.5 V battery, 1.8 V VOUT

When an FET is connected in series with the battery and the battery voltage drops to 0.9 V, the maximum current for the boost is 10 mA. This behavior is similar for the PMOS and NMOS used since they have similar characteristics. The following graphs show this behavior.

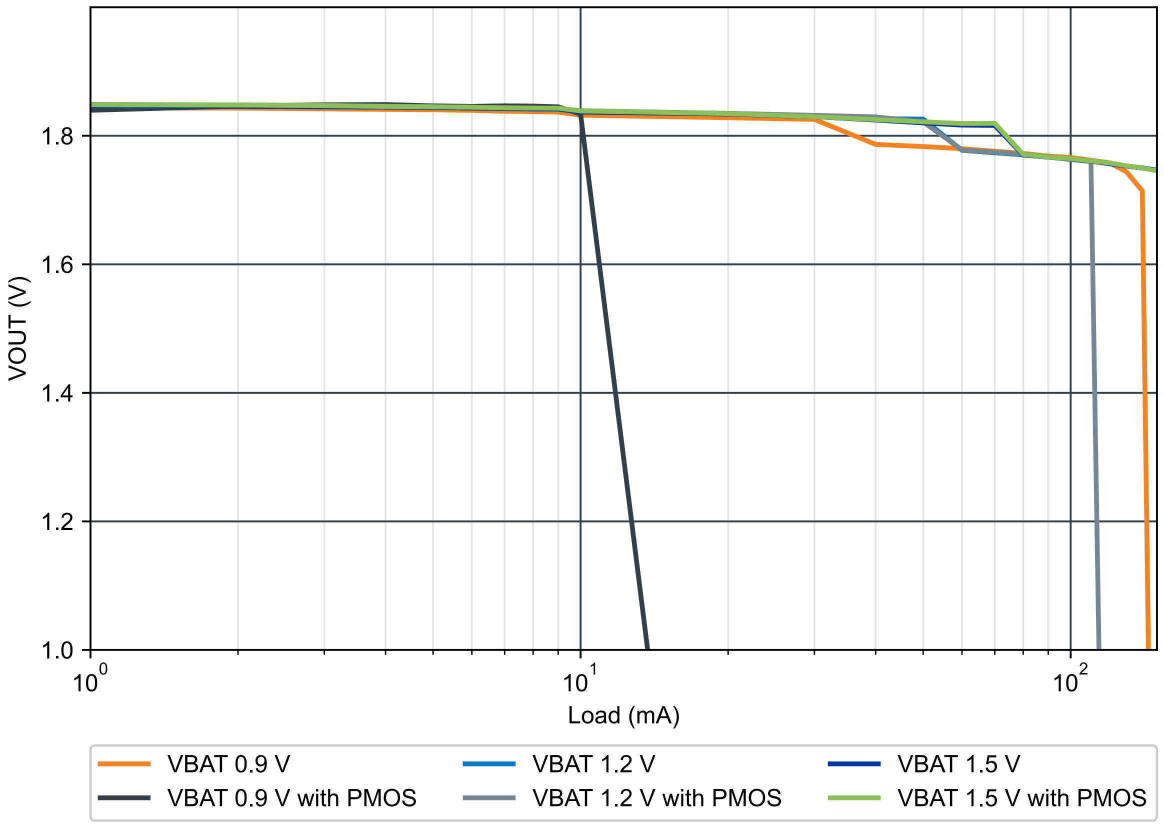

Figure 3: Load regulation comparison of PMOS with 1.5 V battery, 1.8 V VOUT

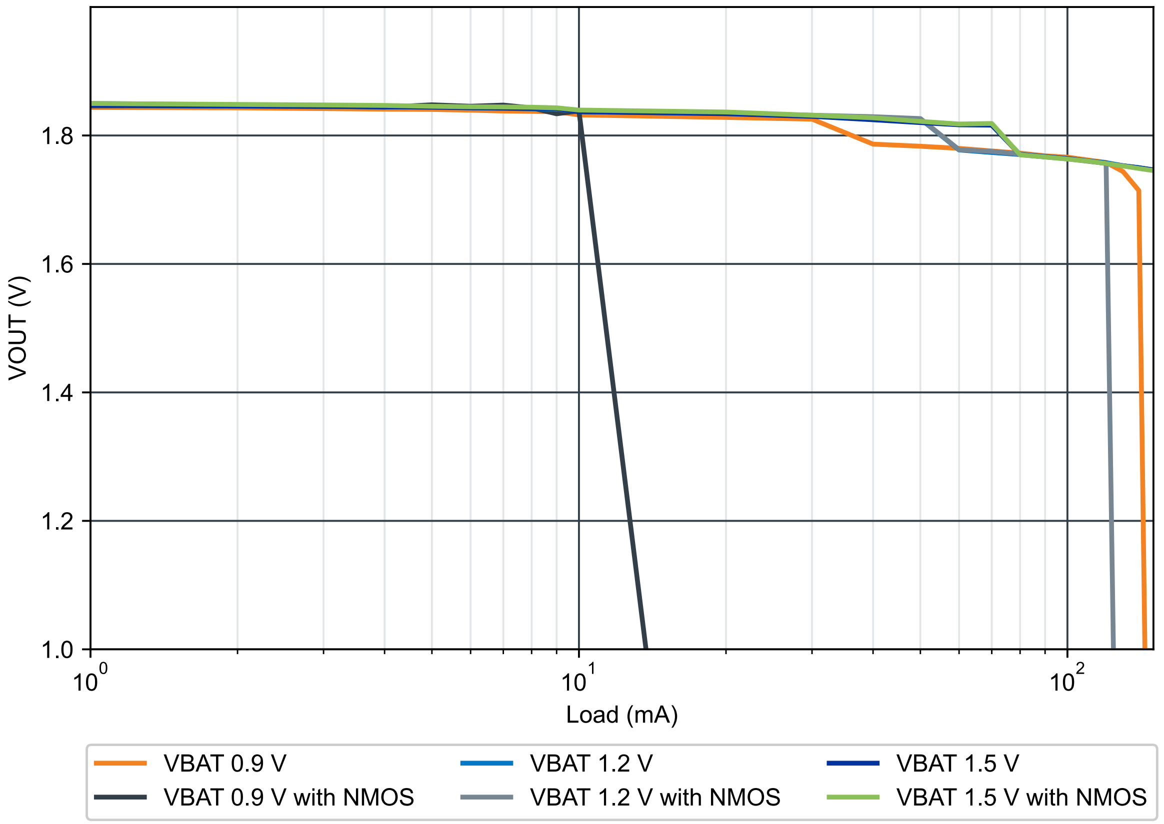

Figure 4: Load regulation comparison for NMOS with 1.5 V battery, 1.8 V VOUT

Operating close to the minimum supply voltage of 0.9 V impacts system efficiency. When the battery is full, this impact is almost negligible.

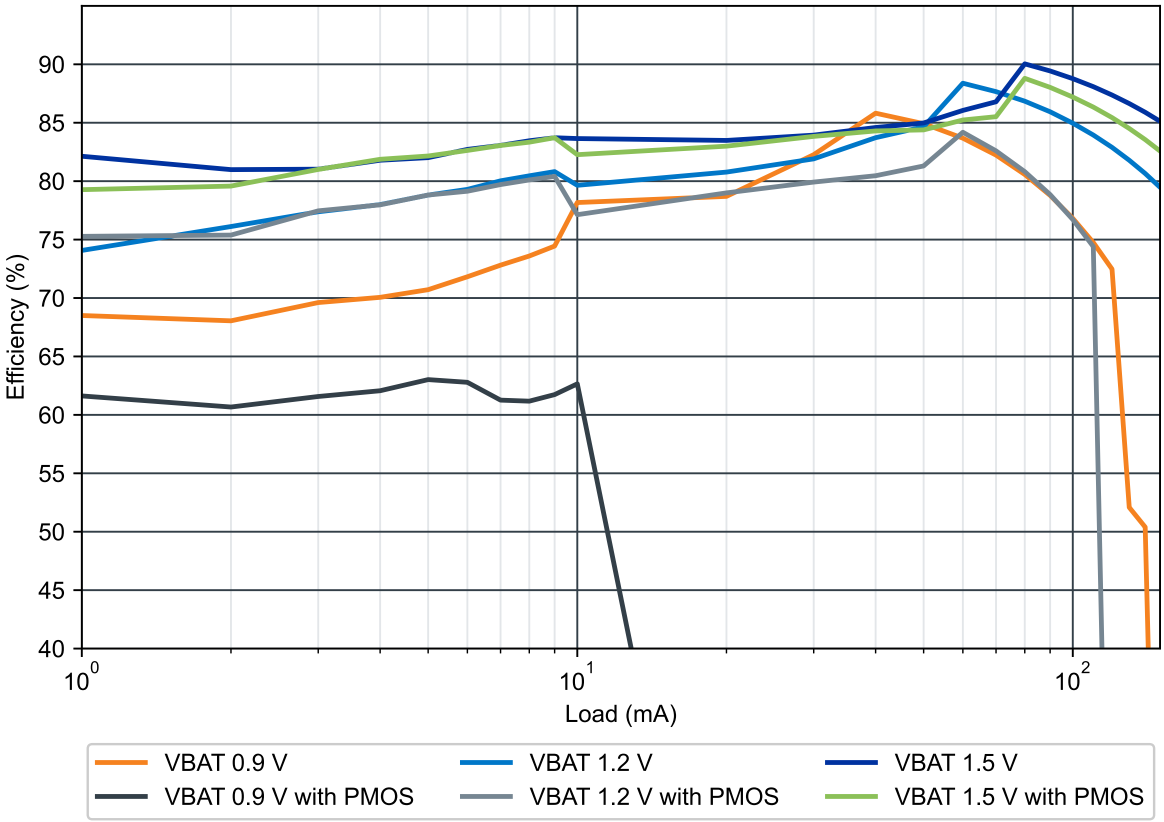

Figure 5: Efficiency comparison of PMOS with 1.5 V battery, 1.8 V VOUT

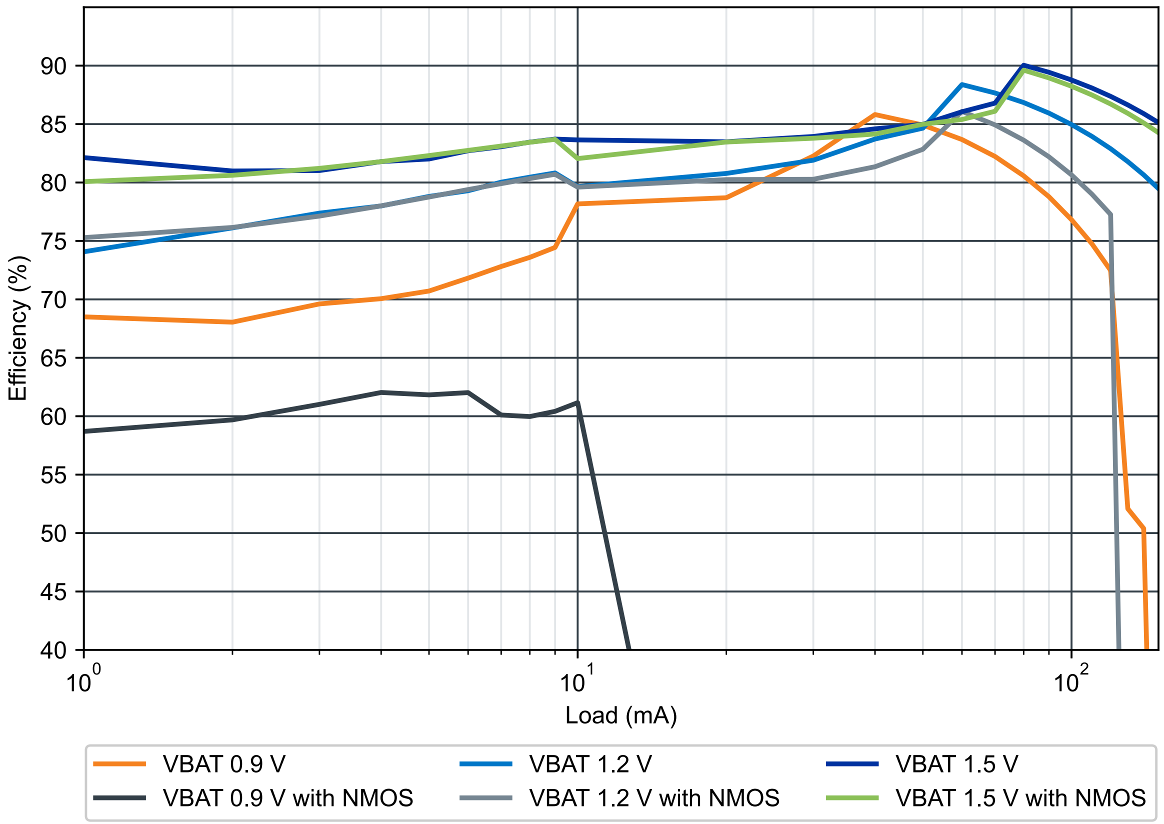

Figure 6: Efficiency comparison of NMOS with 1.5 V battery, 1.8 V VOUT

1.5 V battery, 3 V VOUT

With higher boost output voltage, the maximum current with battery voltage at 0.9 V is even lower. This is expected since the conversion ratio is higher. The effect is much smaller when operating at 1.2 V battery voltage or higher. In this state, the boost is able to support most applications.

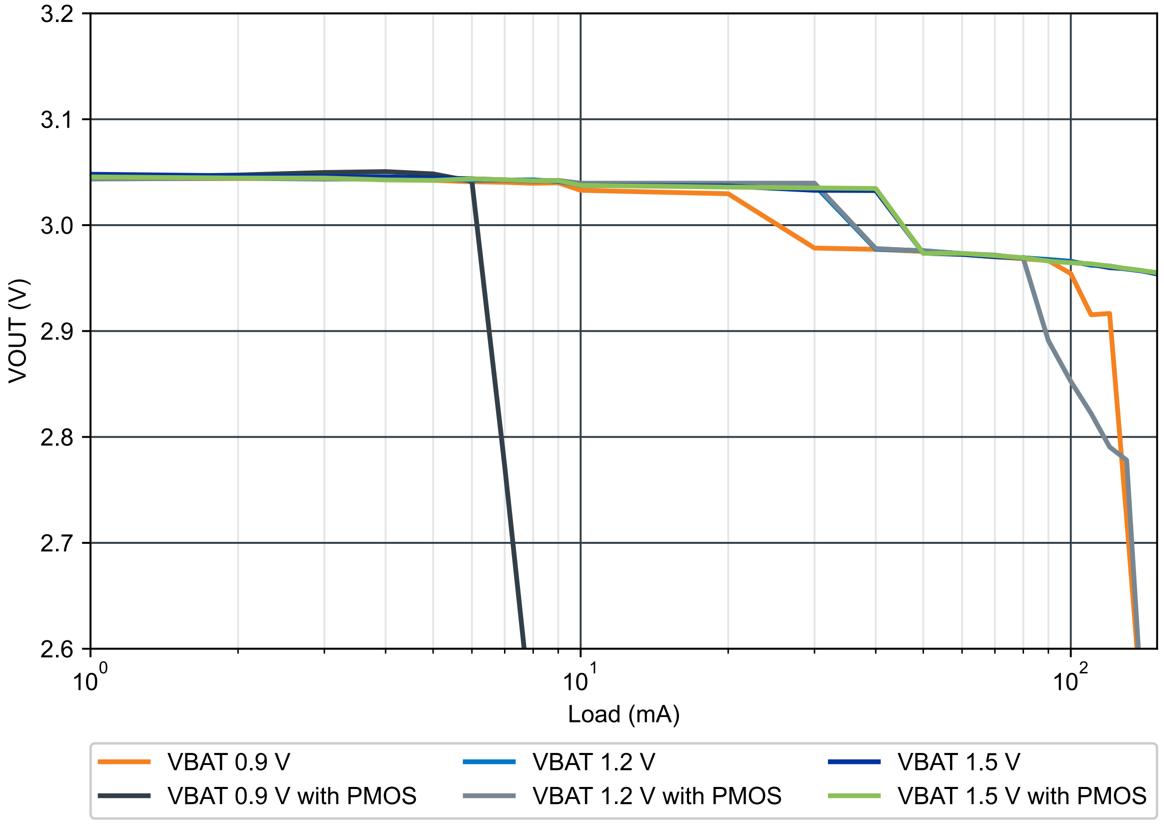

Figure 7: Load regulation comparison of PMOS with 1.5 V battery, 3 V VOUT

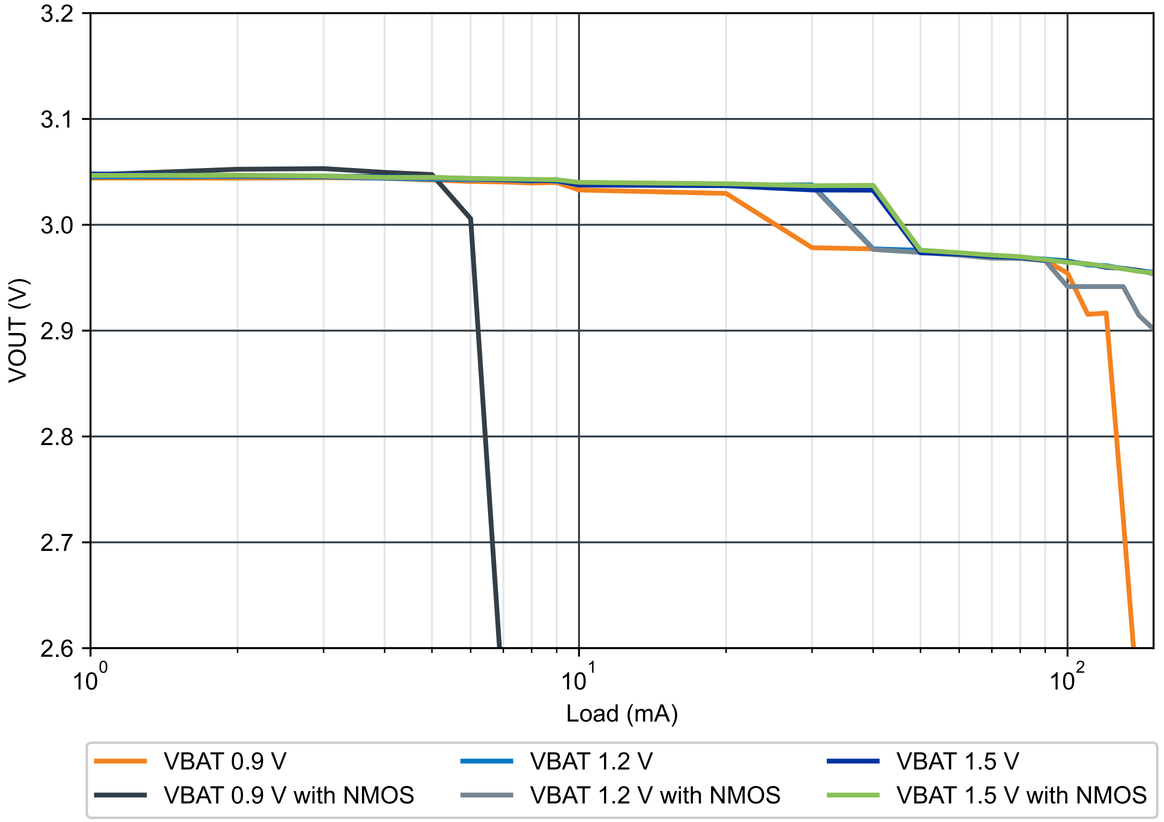

Figure 8: Load regulation comparison of NMOS with 1.5 V battery, 3 V VOUT

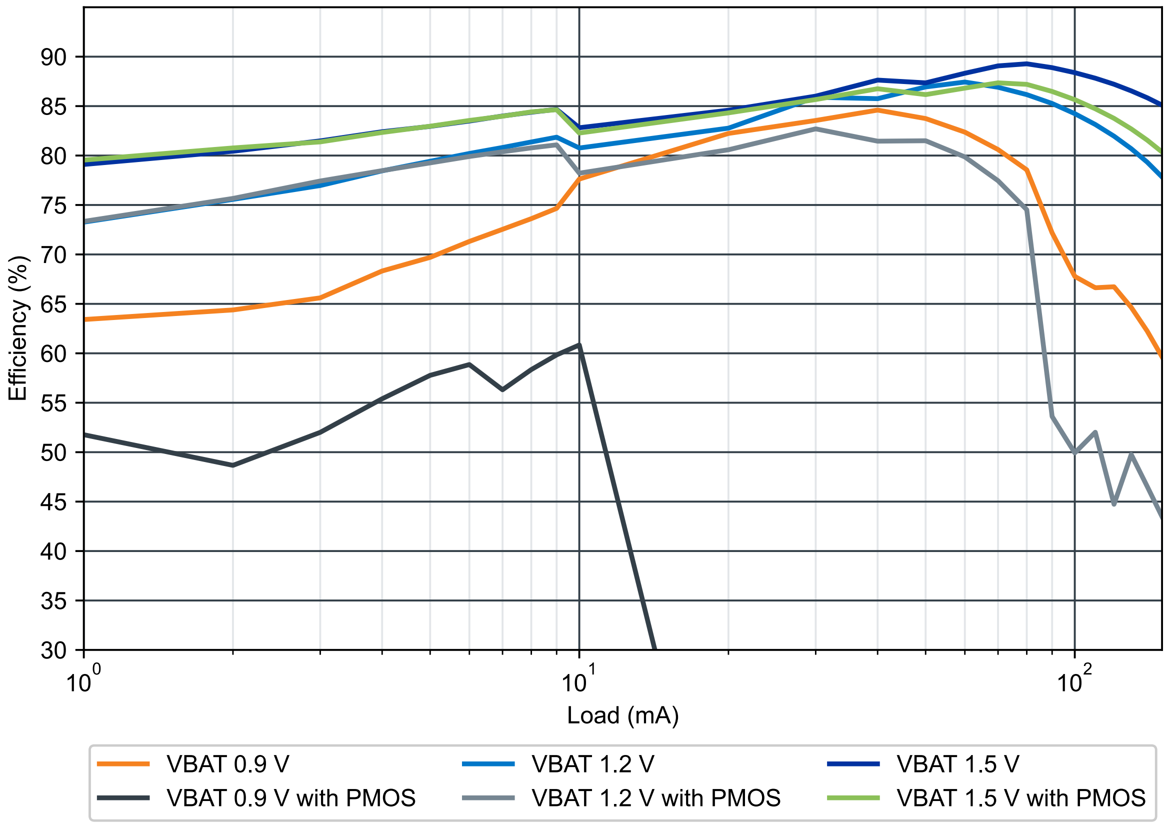

Figure 9: Efficiency comparison of PMOS with 1.5 V battery, 3 V VOUT

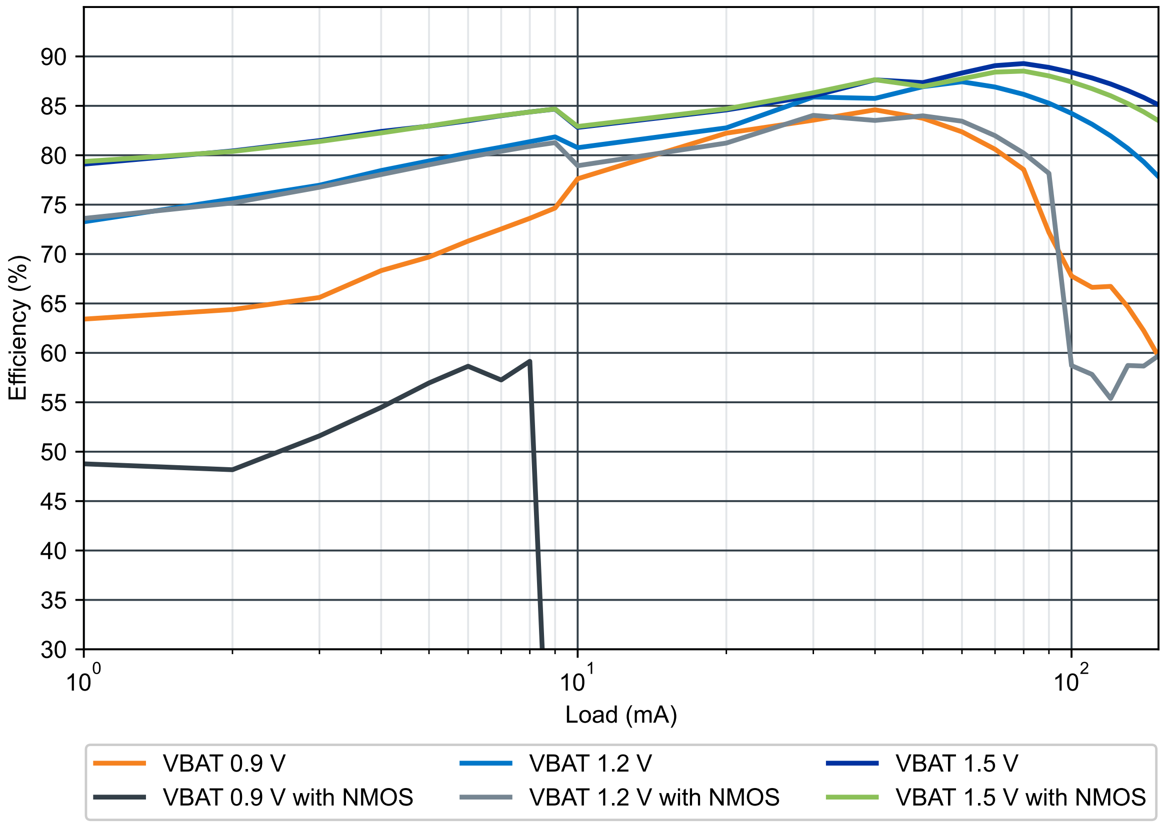

Figure 10: Efficiency comparison of NMOS with 1.5 V battery, 3 V VOUT

3 V battery, 3 V VOUT

When a 3 V battery is used, adding a protection FET has almost no effect on the behavior compared to operating without protection. The protection FET is fully on, and the voltage drop across it is very small.

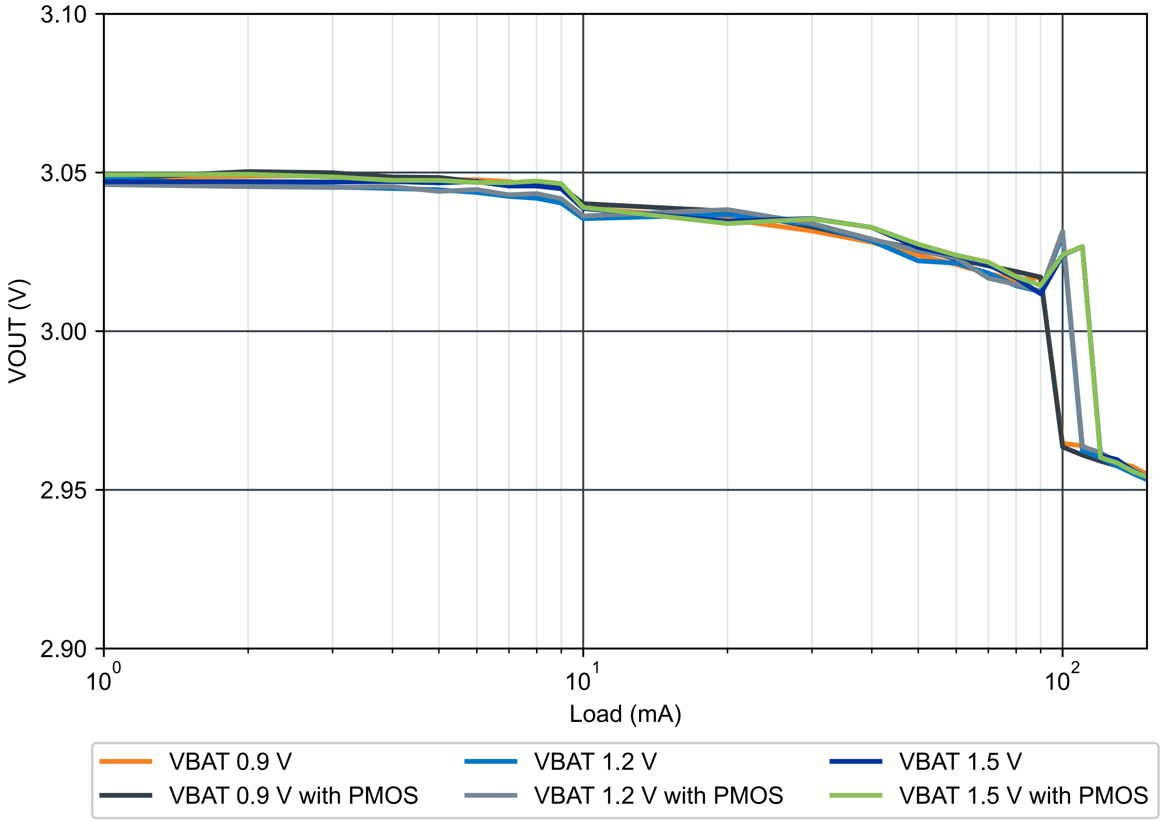

Figure 11: Load regulation comparison of PMOS with 3 V battery, 3 V VOUT

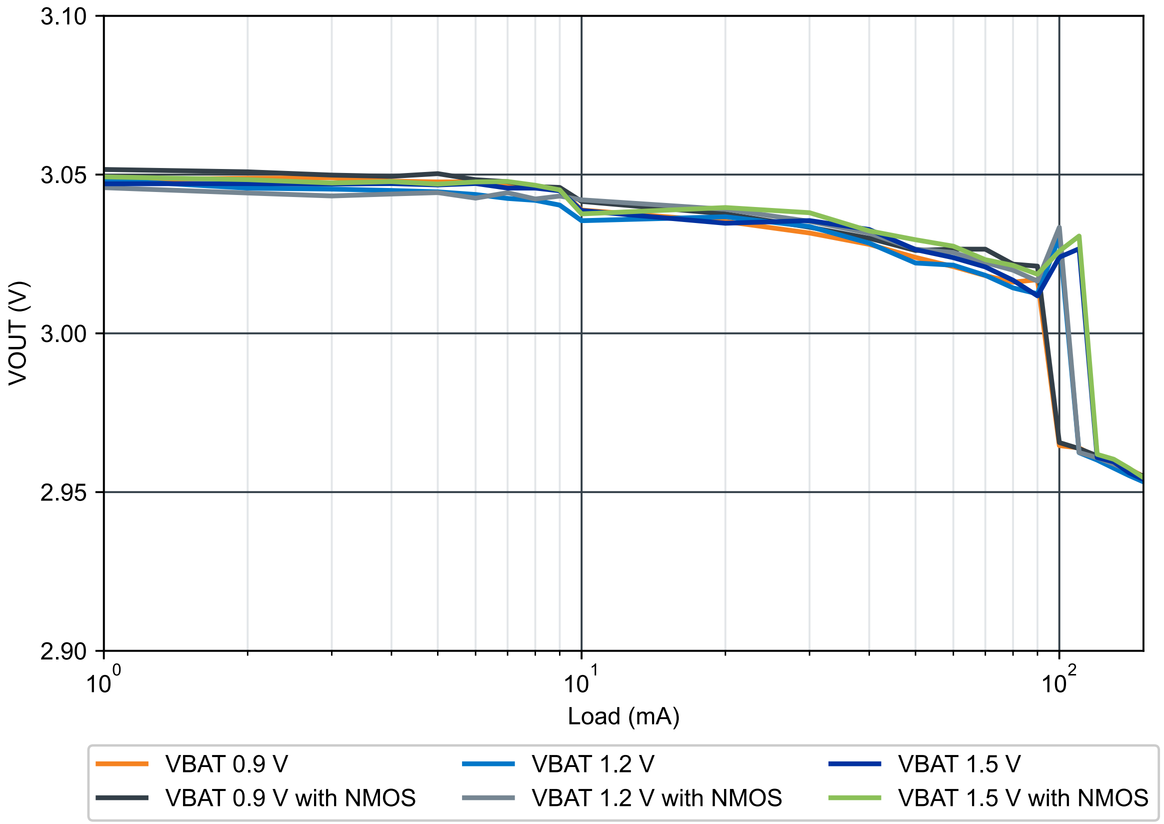

Figure 12: Load regulation comparison of NMOS with 3 V battery, 3 V VOUT

Like with voltage, adding a protection FET has almost no effect on the efficiency.

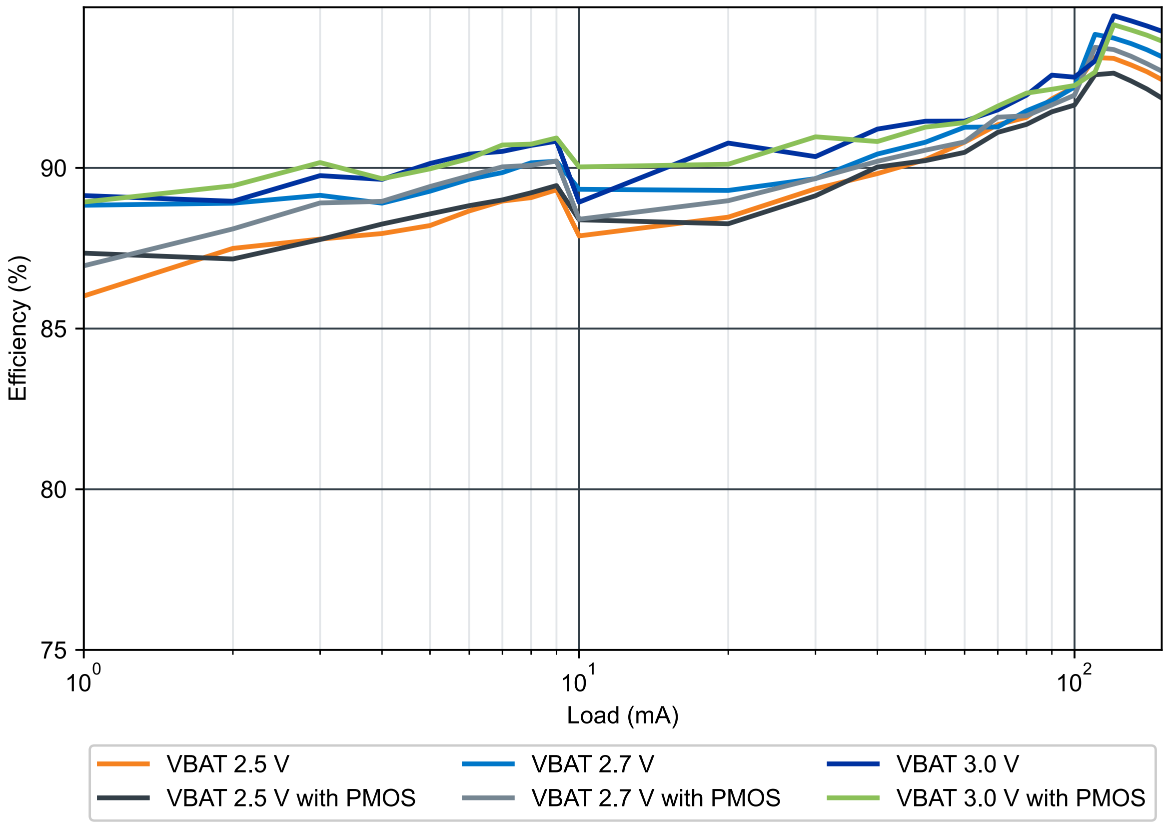

Figure 13: Efficiency comparison of PMOS with 3 V battery, 3 V VOUT

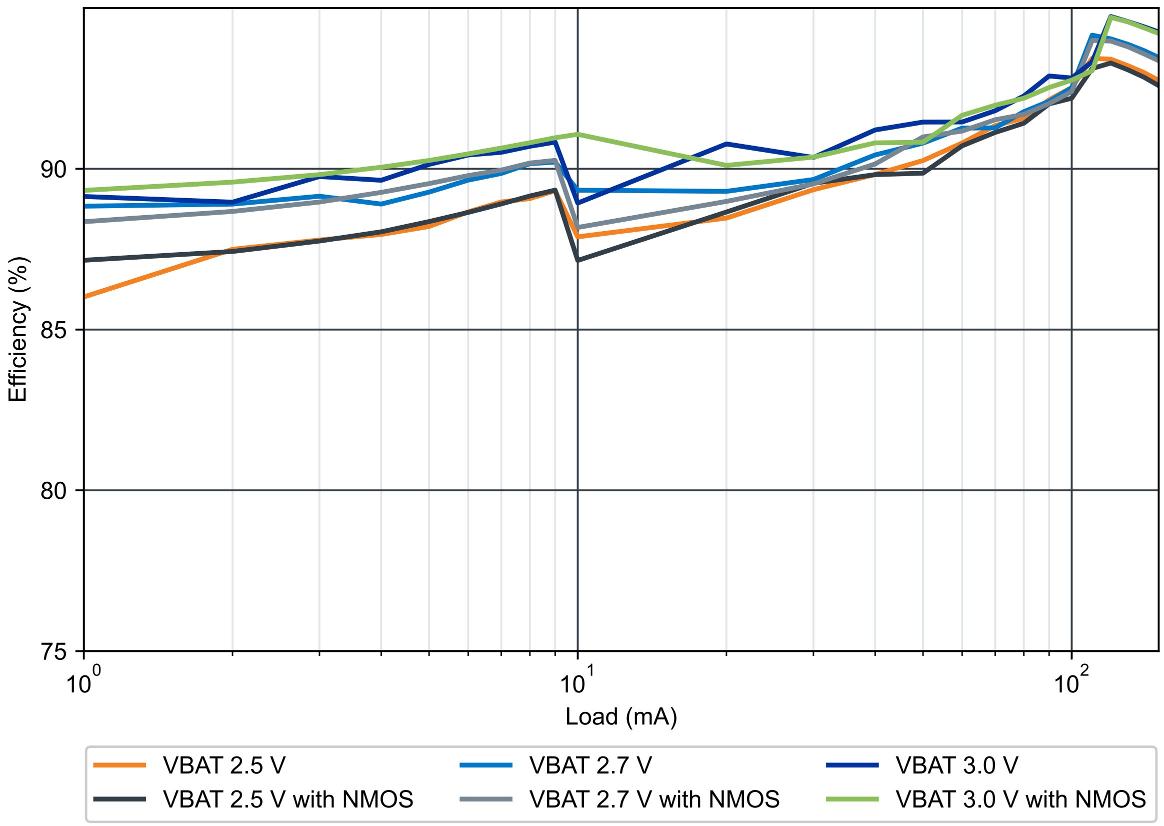

Figure 14: Efficiency comparison of NMOS with 3 V battery, 3 V VOUT

5 Protection with a diode between VBAT and PVSS

An external diode can be used for shunting the reverse current through the external diode instead of the nPM2100 PMIC. Depending on the forward voltage, the current is divided between the external diode and the nPM2100 PMIC.

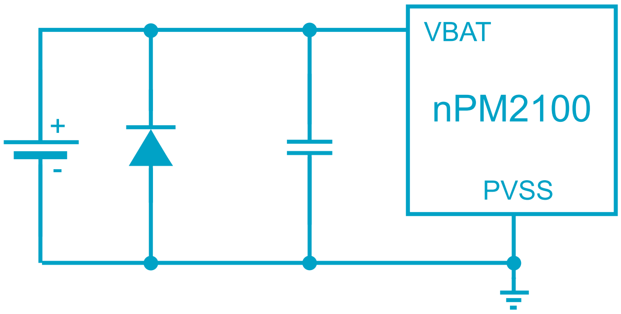

Figure 15: Diode between ***VBAT*** *and* ***PVSS*** *connection diagram*

The diode's forward voltage should be as low as possible. This is to make sure that most of the current goes through the diode instead of the nPM2100 PMIC. This means that a Schottky diode is a good option, though Schottky diodes usually have a relatively high leakage current in the reverse direction. This leakage can impact, for example, the quiescent current for normal operation and ship mode. The selected diode should have low forward voltage and low reverse leakage and be able to withstand high battery current.

Note: A diode between **VBAT** and **PVSS** does not prevent the battery from overheating and potentially being damaged.

6 Protection with a diode in series with VBAT

In normal operation, a diode in series with **`VBAT`** becomes forward-biased, and the current flows through it. When the battery is installed in the reverse polarity, the diode becomes reverse-biased and no current flows.

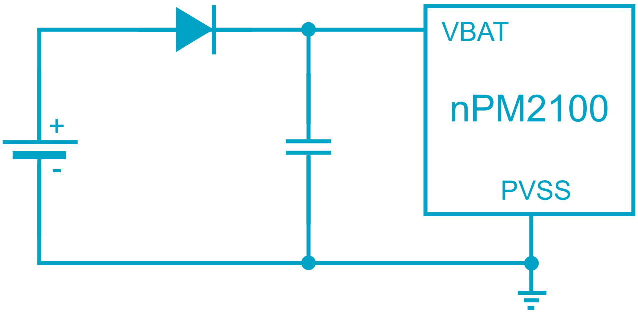

*Figure 16: Diode in series with **`VBAT`** connection diagram*

The forward voltage drop across the diode shortens the usable battery life. For example, an alkaline battery capable of providing 1.5 V is limited to 1.5 V − 0.6 V = 0.9 V. The boost which follows the battery also suffers due to this drop. Because a Schottky diode has a lower forward voltage drop, it can be used instead of a regular diode to minimize these disadvantages.

In practice, this configuration cannot be used with a 1.5 V battery because the voltage drop is too high. This results in a very limited usable voltage range and very poor system efficiency.

Even with a 3 V battery, the efficiency loss is considerable when measured from the supply voltage. For a normal P-N junction diode, the loss is 0.6 V out of 3 V, or 20%. For a Schottky diode, the efficiency loss can be 0.3 V out of 3 V, or 10%.

The selected diode should have a forward current that can support the device in all conditions. It should also have a sufficient voltage rating because leakage current occurs when the battery is installed in reverse polarity. Using a Schottky diode is more expensive than a normal diode, but has a low forward voltage.

7 Protection with an ideal diode

An ideal diode *Integrated Circuit (IC)* acts as a very low ohmic switch when the polarity is correct and protects the device from reverse polarity.

An ideal diode can also be used for switching between batteries when the device has two batteries in parallel. If the ideal diode is placed in series with each battery, it prevents the current flowing between them if they have different voltages.

The supply voltage range typically starts at 1.5 V, so ideal diodes are suitable only for 3 V batteries. Also, the quiescent current of such a device can be significantly higher than the nPM2100 PMIC's current consumption.

8 Summary

Several reverse battery protection methods are presented in this document. The following table summarizes the methods.

Method	**Suitable batteries**	**Impact on efficiency**	**Comment**
PMOS	All	Some impact for 1.5 V batteries	Excellent protection for both the battery and the device.
NMOS	All	Some impact for 1.5 V batteries	Excellent protection for both the battery and the device.
Diode between `VBAT` and `PVSS`	All	No impact	Does not protect the battery.
Diode in series with `VBAT`	3 V batteries	High	Excellent protection for both the battery and the device.
Ideal diode	3 V batteries	Low	Excellent protection for both the battery and the device. Can be used for switching between batteries in parallel configuration.

Table 2: Summary of reverse battery protection methods

Glossary

Electrostatic Discharge (ESD)

A sudden discharge of electric current between two electrically charged objects.

Equivalent Series Resistance (ESR)

A measure of the internal resistance of a battery or capacitor when it is subject to an AC signal. Lower values indicate better performance, allowing for higher currents and reduced energy loss.

Evaluation Kit (EK)

A platform used to evaluate different development platforms.

Field-Effect Transistor (FET)

A type of transistor that controls the flow of current using an electric field. It operates by varying the voltage applied to its gate terminal, which influences the conductivity of a channel between the source and drain terminals.

Integrated Circuit (IC)

A semiconductor chip consisting of fabricated transistors, resistors, and capacitors.

N-Channel Metal-Oxide-Semiconductor (NMOS)

A type of field-effect transistor (FET) used in electronic circuits.

P-Channel Metal-Oxide-Semiconductor (PMOS)

A type of field-effect transistor (FET) used in electronic circuits.

Power Management Integrated Circuit (PMIC)

A chip used for various functions related to power management.

Two-wire Interface (TWI)

An I^2C compatible serial communication protocol that enables devices to exchange data by using a two-wire bus system, allowing multiple devices to be connected and controlled by a master device.

Recommended reading

In addition to the information in this document, you may need to consult other documents.

Nordic documentation

- nPM2100 Datasheet
- nPM2100 EK Hardware
- nPM2100 EK product page

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